HT100 Series DDR4 UDIMM 1Rx8 Datasheet

General Description

This document describes Acer's DDR4 1Rank 8GB/16GB SDRAM Unbuffered DIMM product.

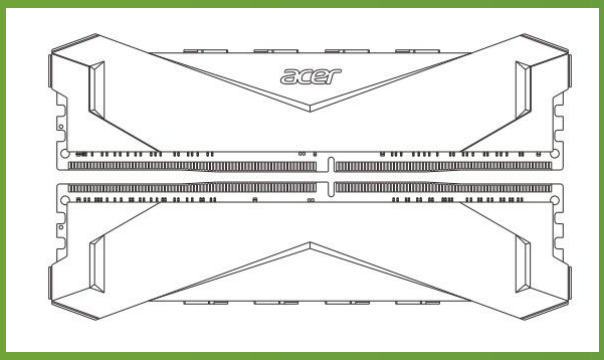
This product design specification reference JEDEC standard (No. 21C DDR4 SDRAM DIMM Design Specification).

This product's PCBA outline reference JEDEC design MO309.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 288-pin, unbuffered dual in-line memory module (UDIMM)
- Equipped with efficient heat sink
- Fast data transfer rates: PC4-2666, PC4-3200
- 8GB (1Gig x 64) ,16GB (2Gig x 64)
- VDD = 1.20V (NOM), VDD = 1.35V (XMP)
- VPP = 2.5V (NOM)
- VDDSPD = 2.5V (NOM)
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die VREFDQ generation and calibration
- Single-rank
- On-board I2 serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control command and address bus

Options



- Operating temperature
  - Commercial (0°C ≤ TOPER ≤ +85°C)
- Storage temperature
  - -55°C ≤ TSTG ≤ +100°C
- Package: 288-pin DIMM (halogen-free)
- Frequency/CAS latency
  - 0.625ns @ CL = 16 (DDR4-3200)
  - 0.750ns @ CL = 18 (DDR4-2666)
  - 0.750ns @ CL = 19 (DDR4-2666)

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1. Ordering Information and Key Features

1) Ordering Information

Acer Model Series	Capacity	Part Number	Data Rate （MT/s)	CL-tRCD-tRP-tRAS	Voltage	tCK(min)
HT100	8GB	BL.9BWWA.231	DDR4-2666	18-18-18-43	1.2V	0.750ns
		BL.9BWWA.234	DDR4-3200（XMP）	16-18-18-38	1.35V	0.625ns
	16GB	BL.9BWWA.237	DDR4-2666	18-18-18-43	1.2V	0.750ns
		BL.9BWWA.241	DDR4-3200（XMP）	16-18-18-38	1.35V	0.625ns

2) Key Features

Speed	DDR4-2666	DDR4-2666	DDR4-3200 （XMP)	Unit
	18-18-18	19-19-19	16-18-18	
Voltage	1.2(±0.6)	1.2(±0.6)	1.35(XMP)	V
tCK (min)	0.75	0.75	0.625	ns
tRCD (min)	13.50	14.25 (13.75) *1	11.25	ns
tRP (min)	13.50	14.25 (13.75) *1	11.25	ns
tRAS (min)	32	32	23.75	ns
tRC (min)	45.5	46.25 (45.75) *1	35	ns

Note :

1. Before purchase and assembly your computer, please consult motherboard and CPU manufacture, review the motherboard and CPU manufacture website, check the hardware Spec, make sure the hardware support the memory module rated speed and latency.
2. Average Refresh Period 7.8us at lower then T_{CASE} 85℃, 3.9us at 85℃< T_{CASE} < 95℃.
3. *1: Down-bin timing, refer to component data sheet Speed Bin Tables for details.

2. Addressing

Parameter	8GB	16GB
Row address	64K A[15:0]	128K A[16:0]
Column address	1K A[9:0]	1K A[9:0]
Device bank address	4 BA[1:0]	4 BA[1:0]
Device bank group address	4 BG[1:0]	4 BG[1:0]
Device configuration	8Gb (1 Gig x 8) 16 banks	16Gb (2 Gig x 8) 16 banks
Module rank address	CS0_n	CS0_n

3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
VDD	VDD supply voltage relative to VSS	–0.4	1.5	V
VDDQ	VDDQ supply voltage relative to VSS	–0.4	1.5	V
VPP	Voltage on VPP pin relative to VSS	–0.4	3	V
VIN, VOUT	Voltage on any pin relative to VSS	–0.4	1.5	V

Symbol	Parameter	Min	Nom	Max	Units
VDD	VDD supply voltage	1.15/1.30	1.2/1.35	1.25/1.4	V
VPP	DRAM activating power supply	2.375	2.5	2.75	V
VREFCA(DC)	Input reference voltage command/ address bus	0.49 × VDD	0.5 × VDD	0.51 × VDD	V
IVTT	Termination reference current from VTT	–750	–	750	mA
VTT	Termination reference voltage (DC) – command/address bus	0.49 × VDD - 20mV	0.5 × VDD	0.51 × VDD + 20mV	V
IIN	Input leakage current; any input excluding ZQ; 0V < VIN < 1.1V	–2.0	–	2	µA
IZQ	Input leakage current; ZQ	–50.0	–	10	µA
IOZpd	Output leakage current; VOUT = VDD; DQ is High-Z	–	–	10	µA
IOZpu	Output leakage current; VOUT = VSS; DQ is High-Z; ODT is disabled with ODT input HIGH	–50.0	–	–	µA
IVREFCA	VREFCA leakage; VREFCA = VDD/2 (after DRAM is initialized)	–2.0	–	2	µA

Notes:

1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
4. VTT termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.
5. Multiply by the number of DRAM die on the module.
6. Tied to ground. Not connected to edge connector.
7. Multiply by the number of module ranks and then times the number of die per package.

4. Architecture

x8 Package Ball out (Top view) : 78 ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c				DM_n/DBI_n TDQS_t	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS	E
F	VDD	ODT1	ODT				CK_t	CK_c	VDD	F
G	VSS	CKE1	CKE				CS_n	CS1_n	TEN	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				A17	A13	VDD	N
	1	2	3	4	5	6	7	8	9	

5. Pin Assignments

288-Pin DDR4 UDIMM Front								288-Pin DDR4 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	NC	37	VSS	73	VDD	109	VSS	145	NC	181	DQ29	217	VDD	253	DQ41
2	VSS	38	DQ24	74	CK0_t	110	DM5_n/ DBI5_n, NC	146	VREFCA	182	VSS	218	CK1_t	254	VSS
3	DQ4	39	VSS	75	CK0_c	111	NC	147	VSS	183	DQ25	219	CK1_c	255	DQS5_c
4	VSS	40	DM3_n/ DBI3_n, NC	76	VDD	112	VSS	148	DQ5	184	VSS	220	VDD	256	DQS5_t
5	DQ0	41	NC	77	VTT	113	DQ46	149	VSS	185	DQS3_c	221	VTT	257	VSS
6	VSS	42	VSS	78	EVENT_n, NF	114	VSS	150	DQ1	186	DQS3_t	222	PARITY	258	DQ47
7	DM0_n/ DBI0_n, NC	43	DQ30	79	A0	115	DQ42	151	VSS	187	VSS	223	VDD	259	VSS
8	NC	44	VSS	80	VDD	116	VSS	152	DQS0_c	188	DQ31	224	BA1	260	DQ43
9	VSS	45	DQ26	81	BA0	117	DQ52	153	DQS0_t	189	VSS	225	A10_AP	261	VSS
10	DQ6	46	VSS	82	RAS_n/ A16	118	VSS	154	VSS	190	DQ27	226	VDD	262	DQ53
11	VSS	47	CB4/ NC	83	VDD	119	DQ48	155	DQ7	191	VSS	227	NC	263	VSS
12	DQ2	48	VSS	84	CS0_n	120	VSS	156	VSS	192	CB5, NC	228	WE_n/ A14	264	DQ49
13	VSS	49	CB0/ NC	85	VDD	121	DM6_n/ DBI6_n, NC	157	DQ3	193	VSS	229	VDD	265	VSS
14	DQ12	50	VSS	86	CAS_n/ A15	122	NC	158	VSS	194	CB1, NC	230	NC	266	DQS6_c
15	VSS	51	DM8_n/ DBI8_n, NC	87	ODT0	123	VSS	159	DQ13	195	VSS	231	VDD	267	DQS6_t
16	DQ8	52	NC	88	VDD	124	DQ54	160	VSS	196	DQS8_c	232	A13	268	VSS
17	VSS	53	VSS	89	CS1_n, NC	125	VSS	161	DQ9	197	DQS8_t	233	VDD	269	DQ55
18	DMI_n/ DBI1_n, NC	54	CB6/ DBI8_n, NC	90	VDD	126	DQ50	162	VSS	198	VSS	234	NC	270	VSS
19	NC	55	VSS	91	ODT1, NC	127	VSS	163	DQS1_c	199	CB7, NC	235	NC	271	DQ51
20	VSS	56	CB2/ NC	92	VDD	128	DQ60	164	DQS1_t	200	VSS	236	VDD	272	VSS
21	DQ14	57	VSS	93	NC	129	VSS	165	VSS	201	CB3, NC	237	NC	273	DQ61
22	VSS	58	RESET_n	94	VSS	130	DQ56	166	DQ15	202	VSS	238	SA2	274	VSS
23	DQ10	59	VDD	95	DQ36	131	VSS	167	VSS	203	CKE1, NC	239	VSS	275	DQ57

5. Pin Assignments

288-Pin DDR4 UDIMM Front								288-Pin DDR4 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
24	VSS	60	CKE0	96	VSS	132	DM7_n/ DBI7_n, NC	168	DQ11	204	VDD	240	DQ37	276	VSS
25	DQ20	61	VDD	97	DQ32	133	NC	169	VSS	205	NC	241	VSS	277	DQS7_c
26	VSS	62	ACT_n	98	VSS	134	VSS	170	DQ21	206	VDD	242	DQ33	278	DQS7_t
27	DQ16	63	BG0	99	DM4_n/ DBI4_n, NC	135	DQ62	171	VSS	207	BG1	243	VSS	279	VSS
28	VSS	64	VDD	100	NC	136	VSS	172	DQ17	208	ALERT_n	244	DQS4_c	280	DQ63
29	DM2_n/ DBI2_n, NC	65	A12/BC_n	101	VSS	137	DQ58	173	VSS	209	VDD	245	DQS4_t	281	VSS
30	NC	66	A9	102	DQ38	138	VSS	174	DQS2_c	210	A11	246	VSS	282	DQ59
31	VSS	67	VDD	103	VSS	139	SA0	175	DQS2_t	211	A7	247	DQ39	283	VSS
32	DQ22	68	A8	104	DQ34	140	SA1	176	VSS	212	VDD	248	VSS	284	VDDSPD
33	VSS	69	A6	105	VSS	141	SCL	177	DQ23	213	A5	249	DQ35	285	SDA
34	DQ18	70	VDD	106	DQ44	142	VPP	178	VSS	214	A4	250	VSS	286	VPP
35	VSS	71	A3	107	VSS	143	VPP	179	DQ19	215	VDD	251	DQ45	287	VPP
36	DQ28	72	A1	108	DQ40	144	NC	180	VSS	216	A2	252	VSS	288	VPP

6. Pin Description

The pin description table below is a comprehensive list of all possible pins for DDR4 modules. All pins listed may not be supported on this module. Seeing the Functional Block Diagram for pins specific to this module.

Symbol	Description
A0–A17	SDRAM address bus （Note： Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs this connection pin is NC.）
BA0, BA1	SDRAM bank select
BG0, BG1	SDRAM bank group select
RAS_n	SDRAM row address strobe （Note： RAS_n is a multiplexed function with A16）
CAS_n	SDRAM column address strobe （Note： CAS_n is a multiplexed function with A15）
WE_n	SDRAM write enable （Note： WE_n is a multiplexed function with A14）
CS0_n, CS1_n	DIMM Rank Select Lines
CKE0, CKE1	SDRAM clock enable lines
ODT0, ODT1	SDRAM on-die termination control lines
ACT_n	SDRAM activate
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
TDQS0_t-TDQS8_t TDQS0_c-TDQS8_c	Dummy loads for mixed populations of x4based and x8 based RDIMMs. Not used on UDIMMs.
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair）

6. Pin Description

Symbol	Description
DM0_n–DM8_n,DBI0_n-DBI8_n	SDRAM data masks/data bus inversion(x8-based x64 DIMMs)
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)
SCL	I^2C serial bus clock for SPD-TSE
SDA	I^2C serial bus data line for SPD-TSE
SA0–SA2	I^2C slave address select for SPD-TSE
PARITY	SDRAM parity input
12V	Optional power Supply on socket but notused on UDIMM
VREFCA	Reference voltage for CA
VSS	Power supply return (ground)
VDDSPD	Serial SPD-TSE positive power supply
ALERT_n	SDRAM ALERT_n
VPP	SDRAM Supply
RESET_n	Set DRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use
NC	No Connect: No on DIMM electrical connection is present.

7. Input / Output Functional Description

Item	Symbol	Type	Function
1	CK0_t, CK0_c CK1_t, CK1_c	Input	Clock: CK_t and CK_ care differential clock inputs. crossing of the positive edge of CK_t and negative edge of CK_c.
2	CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Pre-charge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down Input buffers, excluding CKE, are disabled during Self-Refresh.
3	CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS2_n and CS3_n are not used on UDIMMs.
4	C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code. Not used on UDIMMs.
5	ODT0, ODT1	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM
6	ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15 and A14.
7	RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table.

7. Input / Output Functional Description

Item	Symbol	Type	Function
8	DM_n/DBI_n/TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configuration.TDQS is not valid for UDIMMs.
9	BG0, BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Pre-charge command is being applied. BG0 also determines which mode register is to be access edduring a MRS cycle. x4/x8 SDRAM configurations have BG0 and BG1. x16 based SDRAMs only have BG0.
10	BA0, BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bankan Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
11	A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC n, RAS_n/A16, CAS_n/A15 and WE n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 SDRAM configuration.
12	A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Auto-precharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Auto- precharge; LOW: no Auto-precharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
13	A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
14	RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
15	DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC isenabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
16	DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

7. Input / Output Functional Description

Item	Symbol	Type	Function
17	TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c are not valid for UDIMMs.
18	PARITY	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
19	ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on-going DRAM internal recovery transaction is complete. During Connectivity Test mode, this pin functions as an input. Using this signal or not is dependent on the system.
20	RFU		Reserved for Future Use. No on DIMM electrical connection is present.
21	NC		No Connect: No on DIMM electrical connection is present.
22	VDD1	Supply	Power Supply: 1.2 V +/- 0.06 V
23	VSS	Supply	Ground
24	VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
25	VTT2	Supply	Power Supply for termination of Address, Command and Control, VDD/2.
26	12 V	Supply	12 V supply not used on UDIMMs.
27	VDDSPD	Supply	Power supply used to power the I2C bus on the SPD-TSE.
28	VREFCA	Supply	Reference voltage for CA

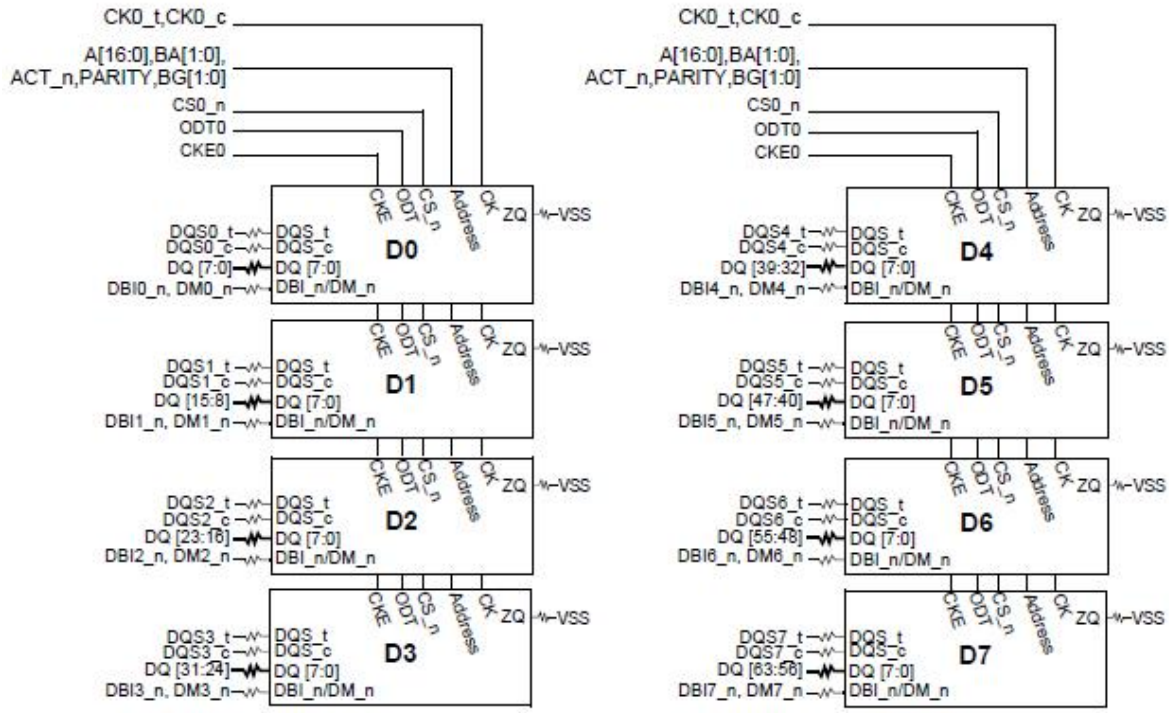
8. DQ Maps

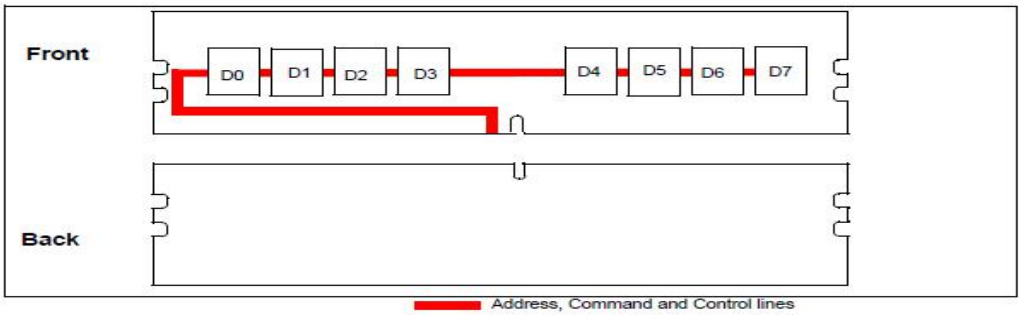
Component-to-Module DQ Map

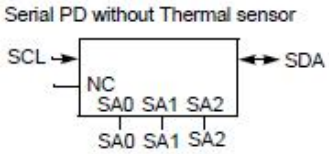
Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
D0	0	3	157	D1	0	11	168
	1	1	150		1	9	161
	2	2	12		2	10	23
	3	0	5		3	8	16
	4	7	155		4	15	166
	5	5	148		5	13	159
	6	6	10		6	14	21
	7	4	3		7	12	14
D2	0	19	179	D3	0	27	190
	1	17	172		1	25	183
	2	18	34		2	26	45
	3	16	27		3	24	38
	4	23	177		4	31	188
	5	21	170		5	29	181
	6	22	32		6	30	43
	7	20	25		7	28	36
D4	0	35	249	D5	0	43	260
	1	33	242		1	41	253
	2	34	104		2	42	115
	3	32	97		3	40	108
	4	39	247		4	47	258
	5	37	240		5	45	251
	6	38	102		6	46	113
	7	36	95		7	44	106
D6	0	51	271	D7	0	59	282
	1	49	264		1	57	275
	2	50	126		2	58	137
	3	48	119		3	56	130
	4	55	269		4	63	280
	5	53	262		5	61	273
	6	54	124		6	62	135
	7	52	117		7	60	128

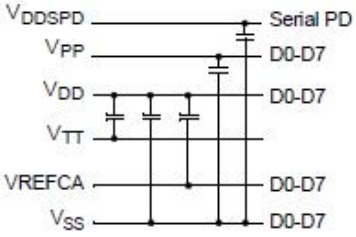
9. Functional Block Diagram

8GB/16GB Non ECC Module (Populated as 1 ranks of x8 DDR4 SDRAMS)



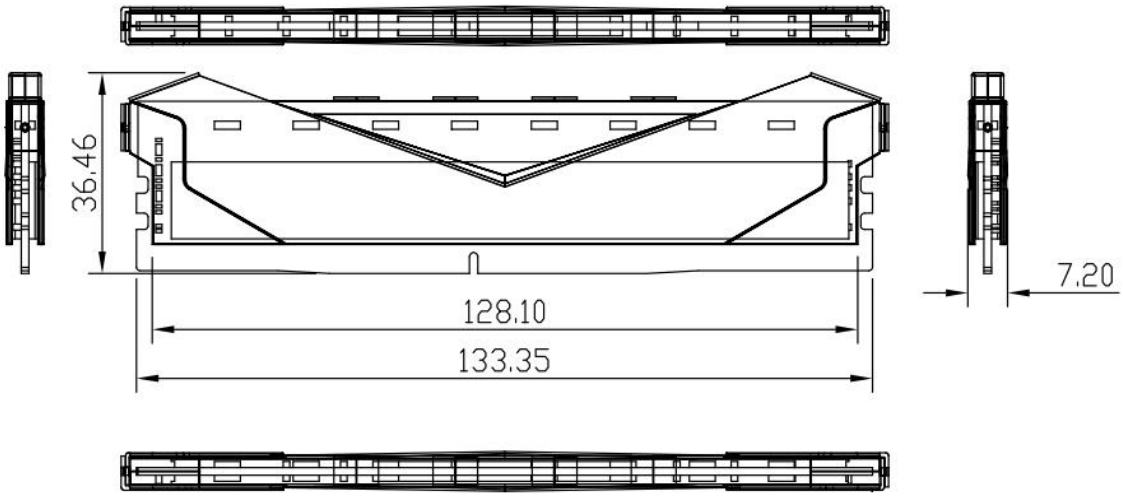




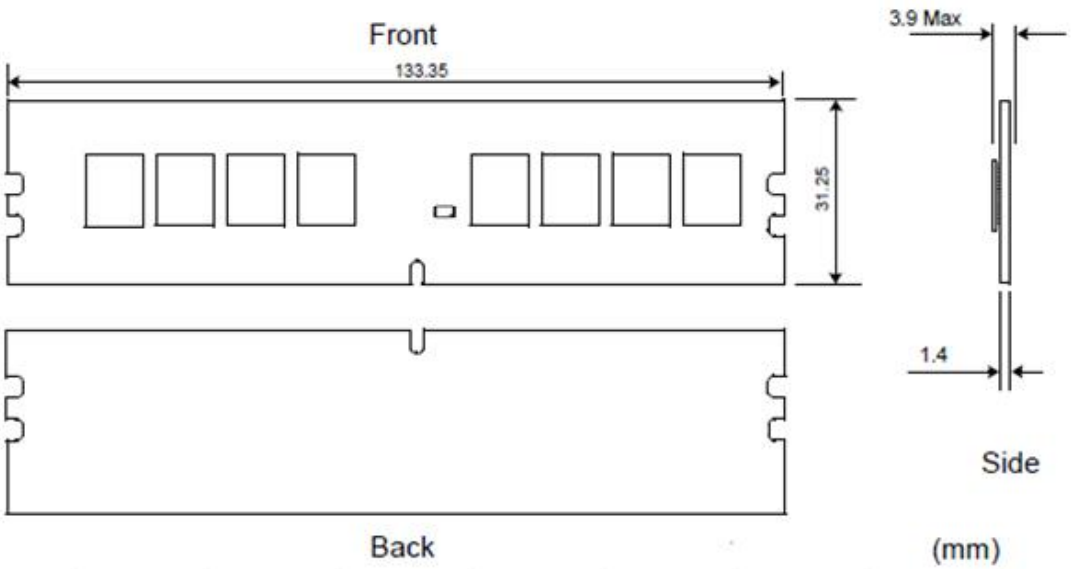


10. Module Dimensions

1Gigx8/2Gigx8*8pcs Module (1 Rank) Physical dimensions:



PCBA Dimensions



Notes:

1. All dimensions are in millimeters.
2. The dimensional diagram is for reference only.

11. Revision History

Date	Revision	Description
Oct-2020	V1.0	Initial release